(12) UK Patent Application (19) GB (11) 2 287 370 (13) A

(43) Date of A Publication 13.09.1995

(21) Application No 9315333.6

(22) Date of Filing 23.07.1993

(51) INT CL[6]
H03F 3/45 1/32

(52) UK CL (Edition N)
H3W WUL
H3T T2T3B T3F T4E1N T6PX

(56) Documents Cited
GB 2059207 A GB 1572079 A EP 0259029 A2
US 4720685 A US 4146844 A

(58) Field of Search
UK CL (Edition L) H3W WUL WVP
INT CL[5] H03F 1/32
ONLINE DATABASES: WPI, INSPEC

(71) Applicant(s)
Gould Instrument Systems Inc

(Incorporated in USA - Ohio)

8333 Rockside Road, Valley View, Ohio,
United States of America

(72) Inventor(s)
Leslie Owen Green

(74) Agent and/or Address for Service
D Young & Co
21 New Fetter Lane, LONDON, EC4A 1DA,
United Kingdom

(54) Amplifier circuit with feed-forward linearity correction

(57) A differential amplifier with feed-forward linearity correction is provided, including a main amplifier 22 having a pair of first amplifying devices configured as a differential pair to provide a differential output based on a differential input; a pair of correction amplifiers 23, 24, each for respectively monitoring a characteristic of one of the main amplifying devices and for providing a linearity correction signal to the differential output as a function of the characteristic; and wherein each of the correction amplifiers includes a pair of second amplifying devices configured as another differential pair, the another differential pair including an input for monitoring the respective characteristic and an output for providing the linearity correction signal. In addition, an amplifier is provided including an amplifier with feed-forward linearity correction, comprising a main amplifier including an amplifying device for providing an amplified output based on an input signal; a correction amplifier for monitoring a characteristic of the amplifying device and for providing a linearity corr ction signal to the output as a function of the characteristic; and wherein the correction amplifier includes a pair of second amplifying devices configured as a differential pair, the differential pair including an input for monitoring the characteristic and an output for providing the linearity correction signal.

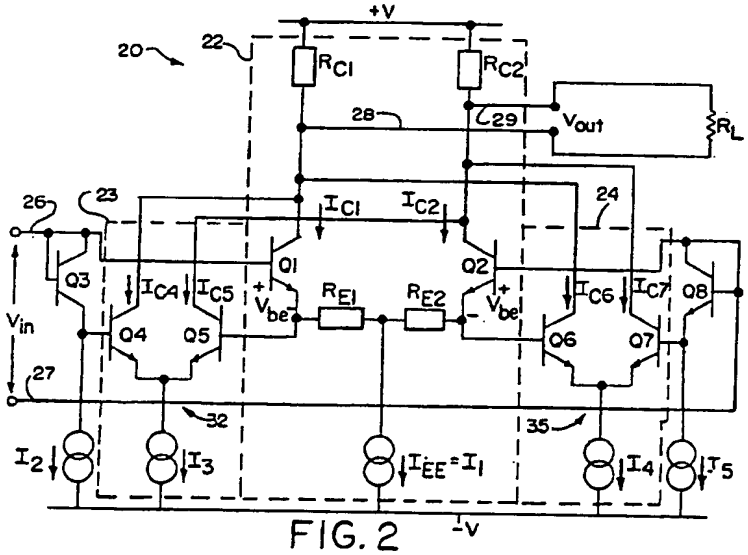
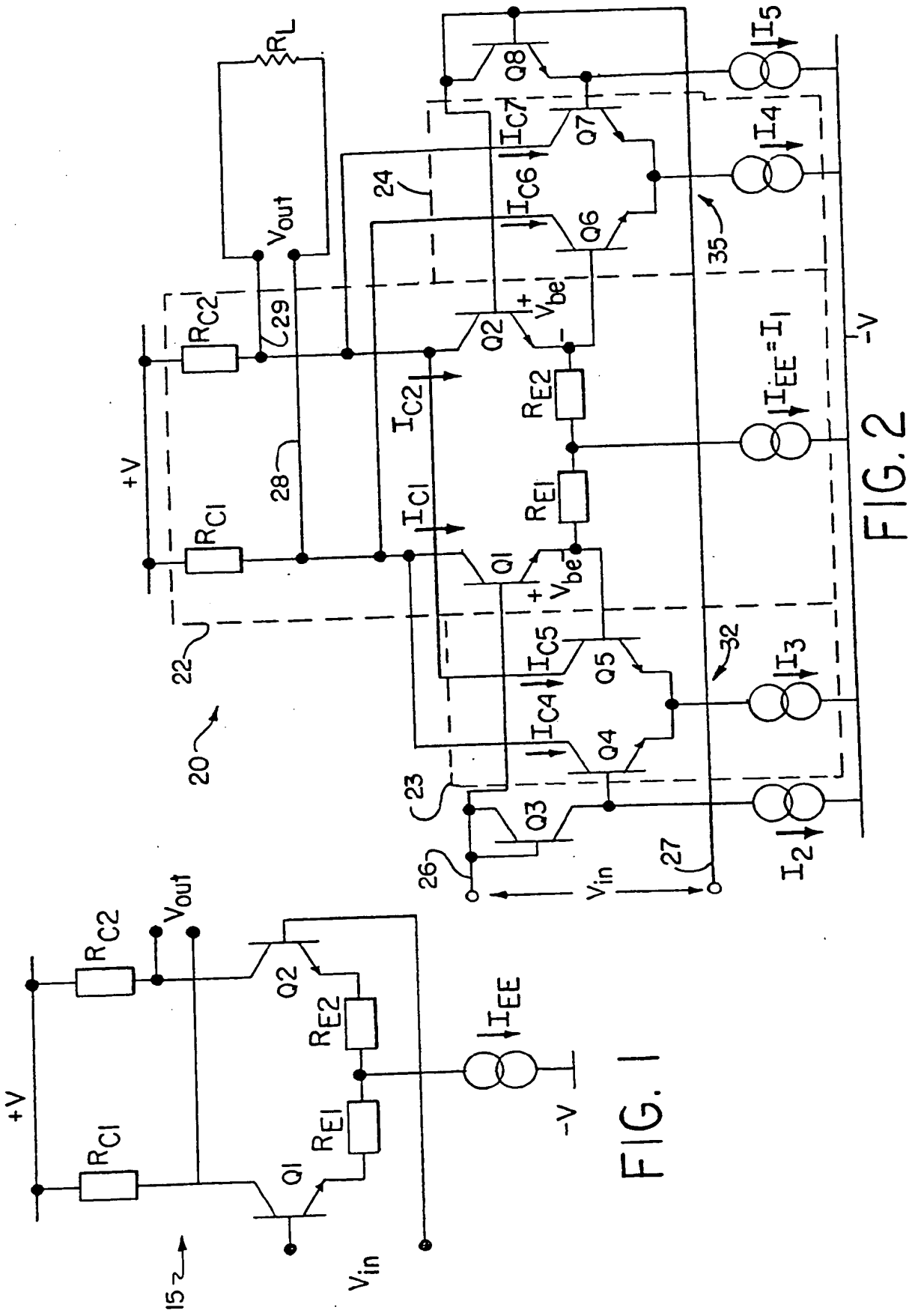


FIG. 2

At least one drawing originally filed was informal and the print reproduced here is taken from a later filed formal copy.

The print reflects an assignment of the application under the provisions of Section 30 of the Patents Act 1977.

GB 2 287 370 A


+V
RC1
RC2
Vout
Q1
Q2
RE1
RE2
IEE
-V
Vin
15
FIG. 1
RL
Q8
Q7
Q6
Q5
Q4
Q3
Q2
Q1
IC7
IC6
IC5
IC4
IC2
IC1
Vbe
I5
I4
I3
I2
IEE=I1
24
135
29
28
22
20
32
23
26
27
FIG. 2

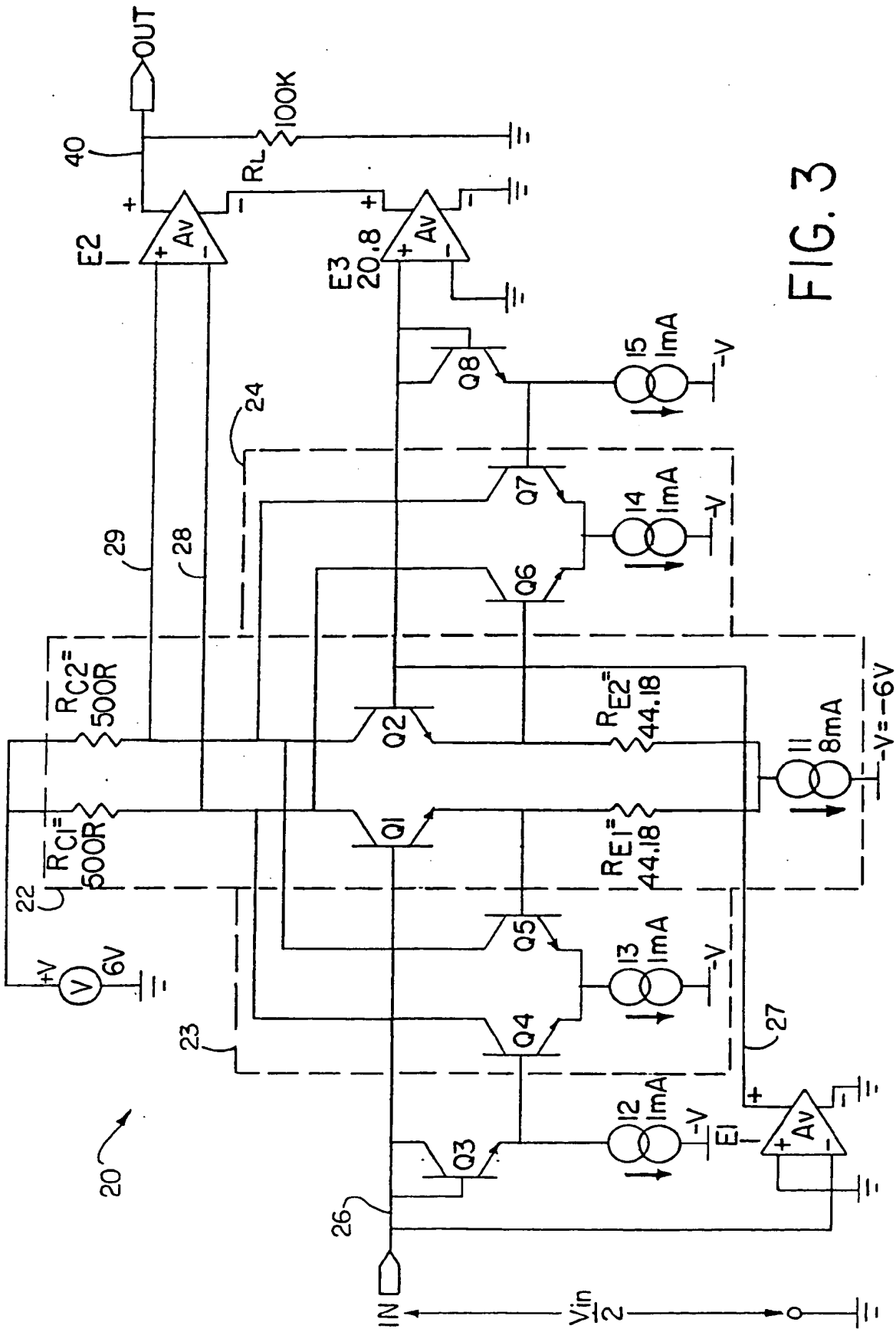

OUT
100K
R_L
40
E2
E3
20.8
Av
Q8
15
1mA
-V
24
Q7
14
Q6
29
28
R_{C2}=
500R
Q2
R_{E2}=
44.18
11
8mA
-V=-6V
R_{C1}=
500R
Q1
R_{E1}=
44.18
22
+V
6V
Q5
13
Q4
23
27
12
Q3
E1
20
26
IN
$\frac{V_{in}}{2}$

FIG. 3

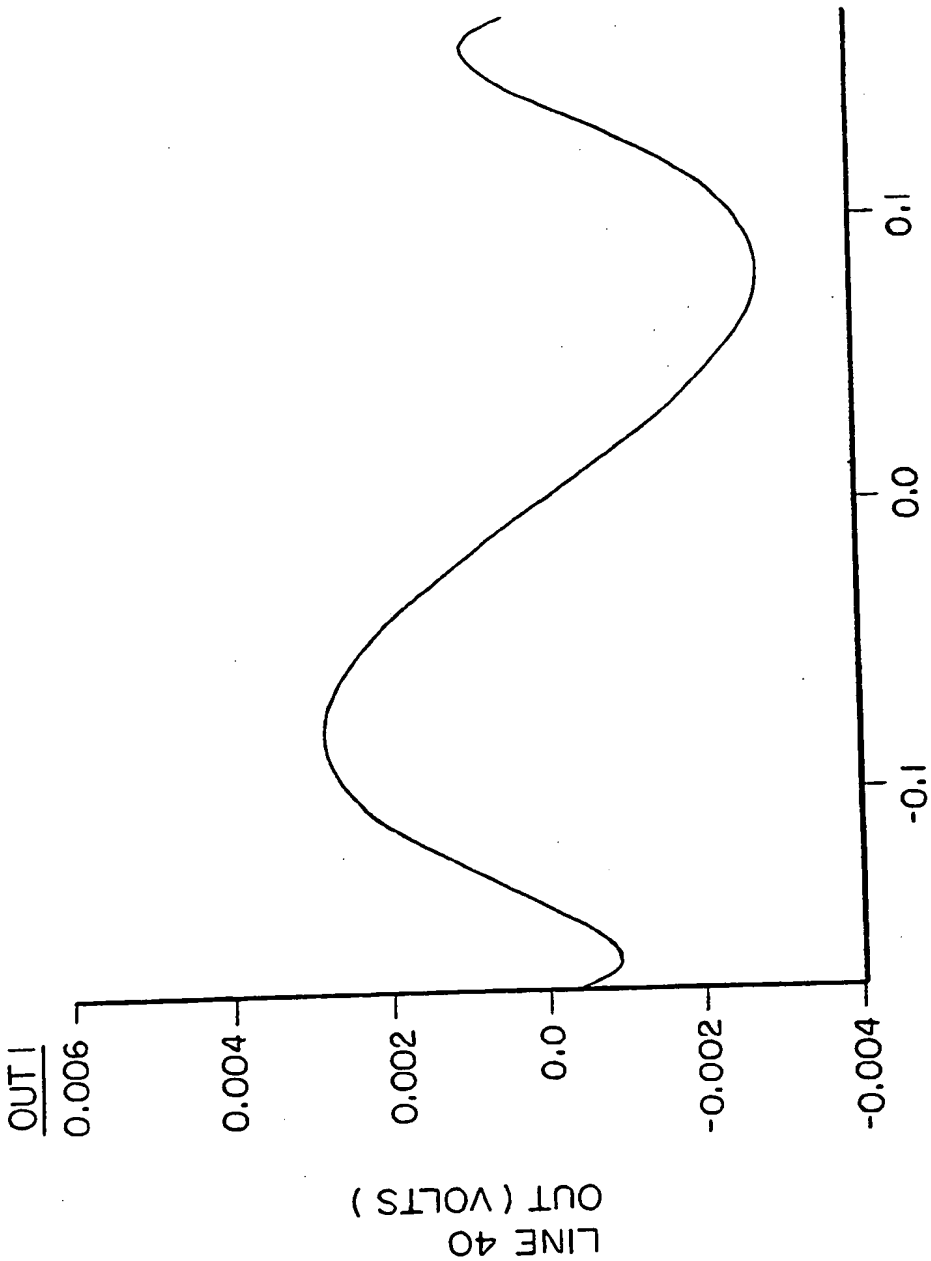

LINE 40
OUT (VOLTS)
OUT I
0.006
0.004
0.002
0.0
-0.002
-0.004
-0.1
0.0
0.1
$\frac{V_{IN}}{2}$ (VOLTS)

FIG. 4

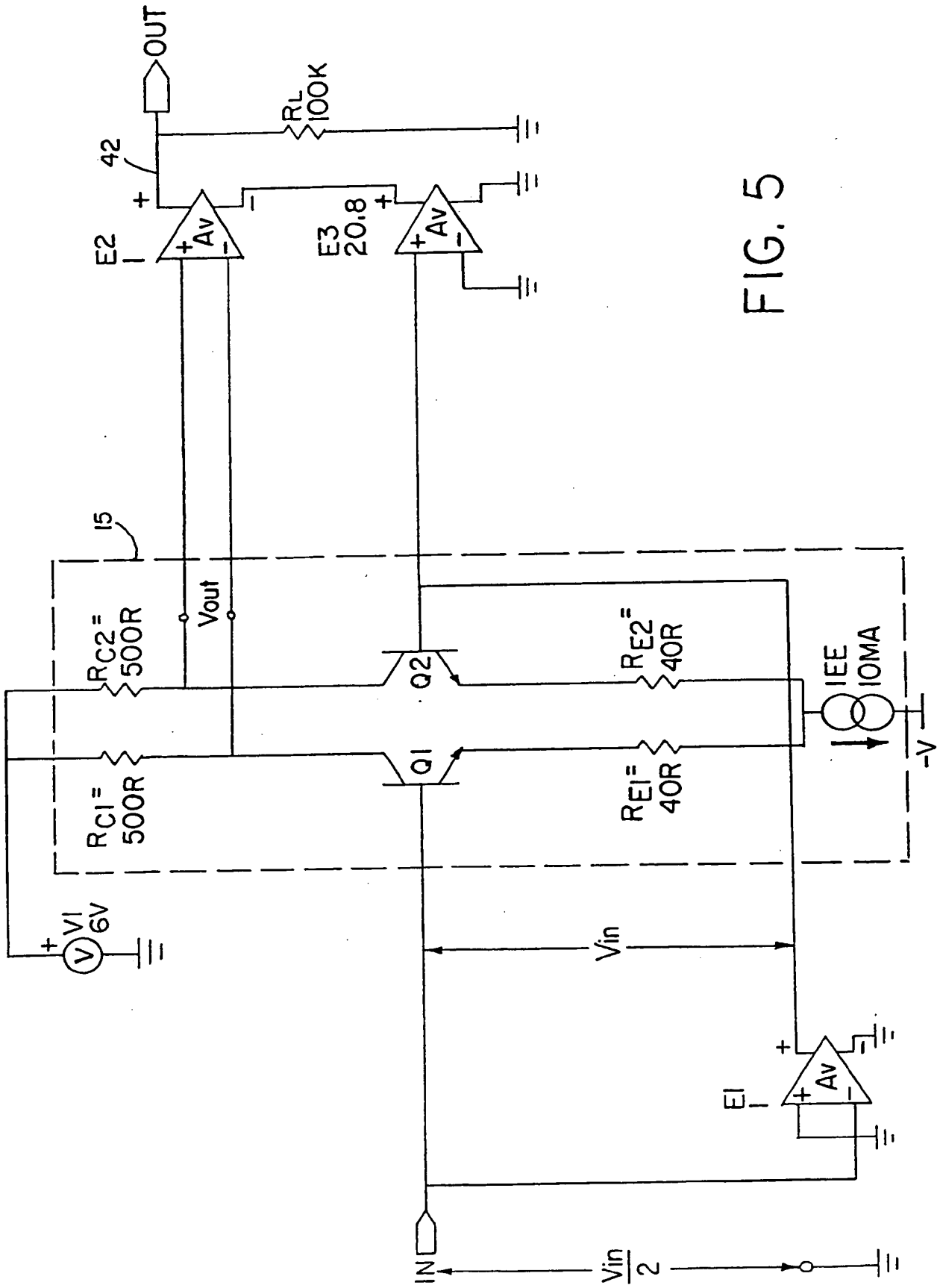

OUT
RL
100K
42
E2
1
Av
E3
20.8
Av
15
Vout
RC2=
500R
RC1=
500R
Q2
Q1
RE2=
40R
RE1=
40R
IEE
10MA
-V
V1
6V
Vin
E1
Av
IN
Vin
2

FIG. 5

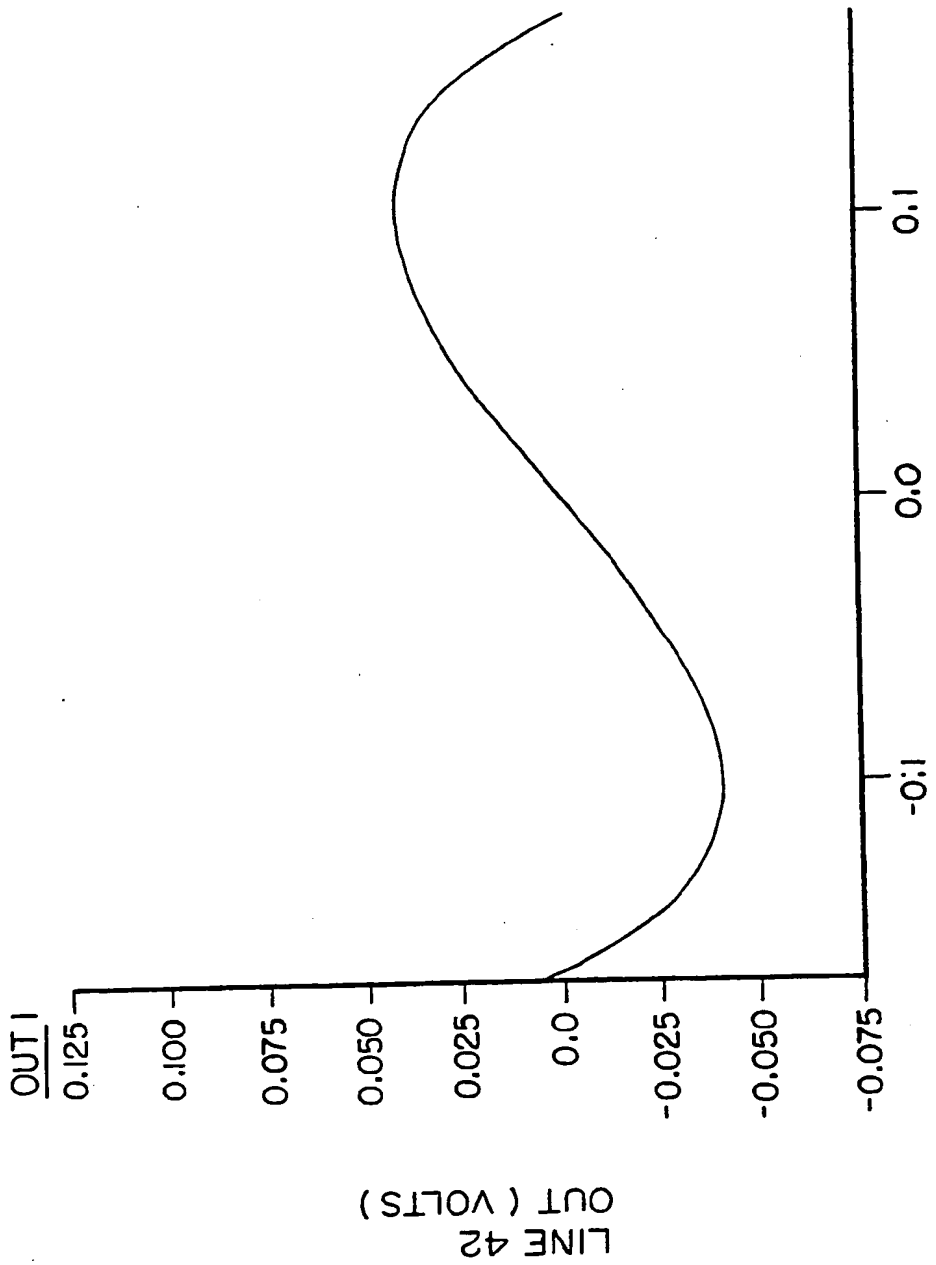

LINE 42
OUT (VOLTS)
OUT I
0.125
0.100
0.075
0.050
0.025
0.0
-0.025
-0.050
-0.075
-0.1
0.0
0.1
$V_{\frac{IN}{2}}$ (VOLTS)

FIG. 6

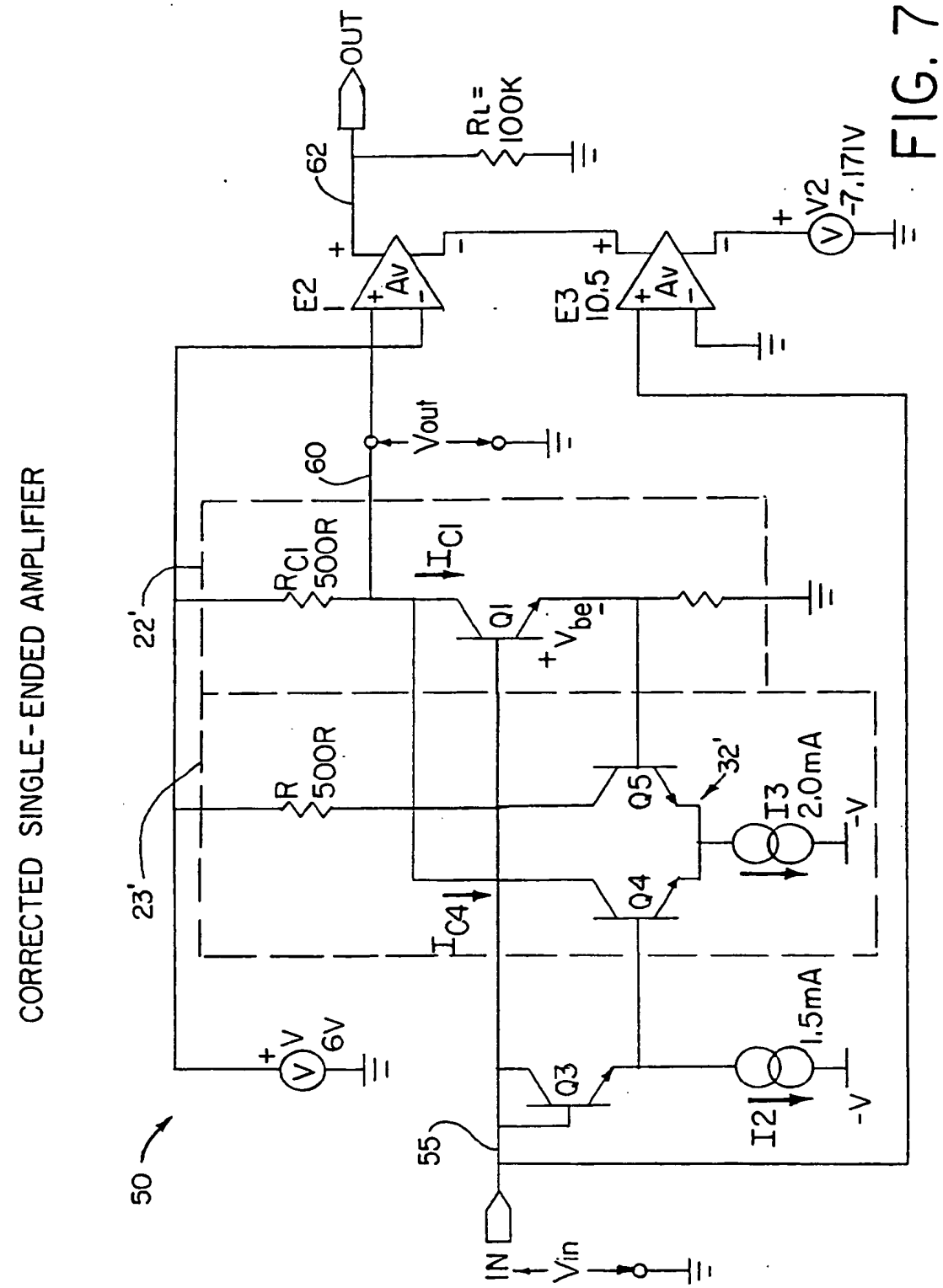

CORRECTED SINGLE-ENDED AMPLIFIER
50
IN
Vin
55
OUT
62
RL=
100K
E2
Av
E3
10.5
V2
-7.171V
Vout
60
22'
23'
RCI
500R
ICI
Q1
+Vbe-
R
500R
Q5
32'
I3
2.0mA
-V
Q4
IC4
V
6V
Q3
I2
1.5mA
-V

FIG. 7

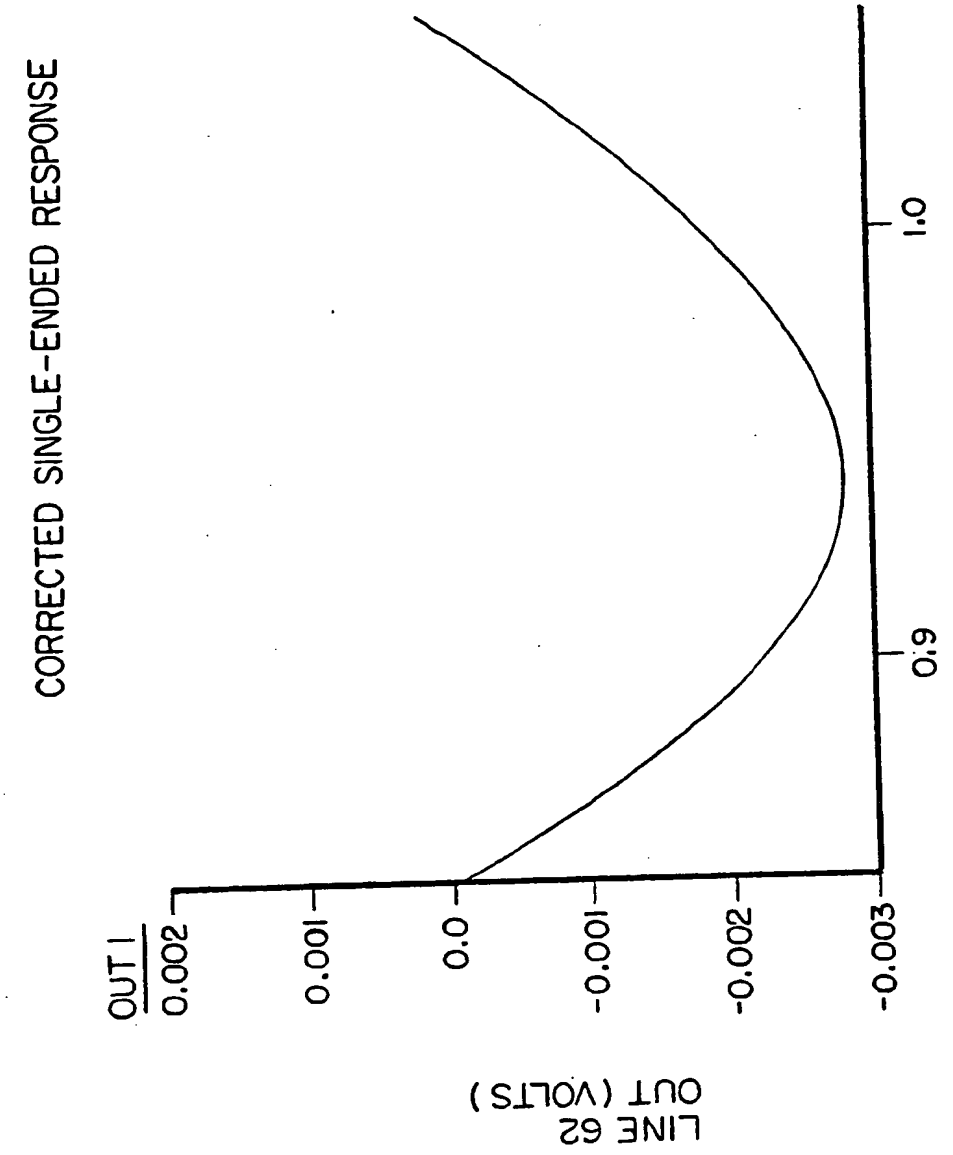

CORRECTED SINGLE-ENDED RESPONSE
OUT 1
0.002
0.001
0.0
-0.001
-0.002
-0.003
0.9
1.0
V_{IN} (VOLTS)
LINE 62
OUT (VOLTS)

FIG. 8

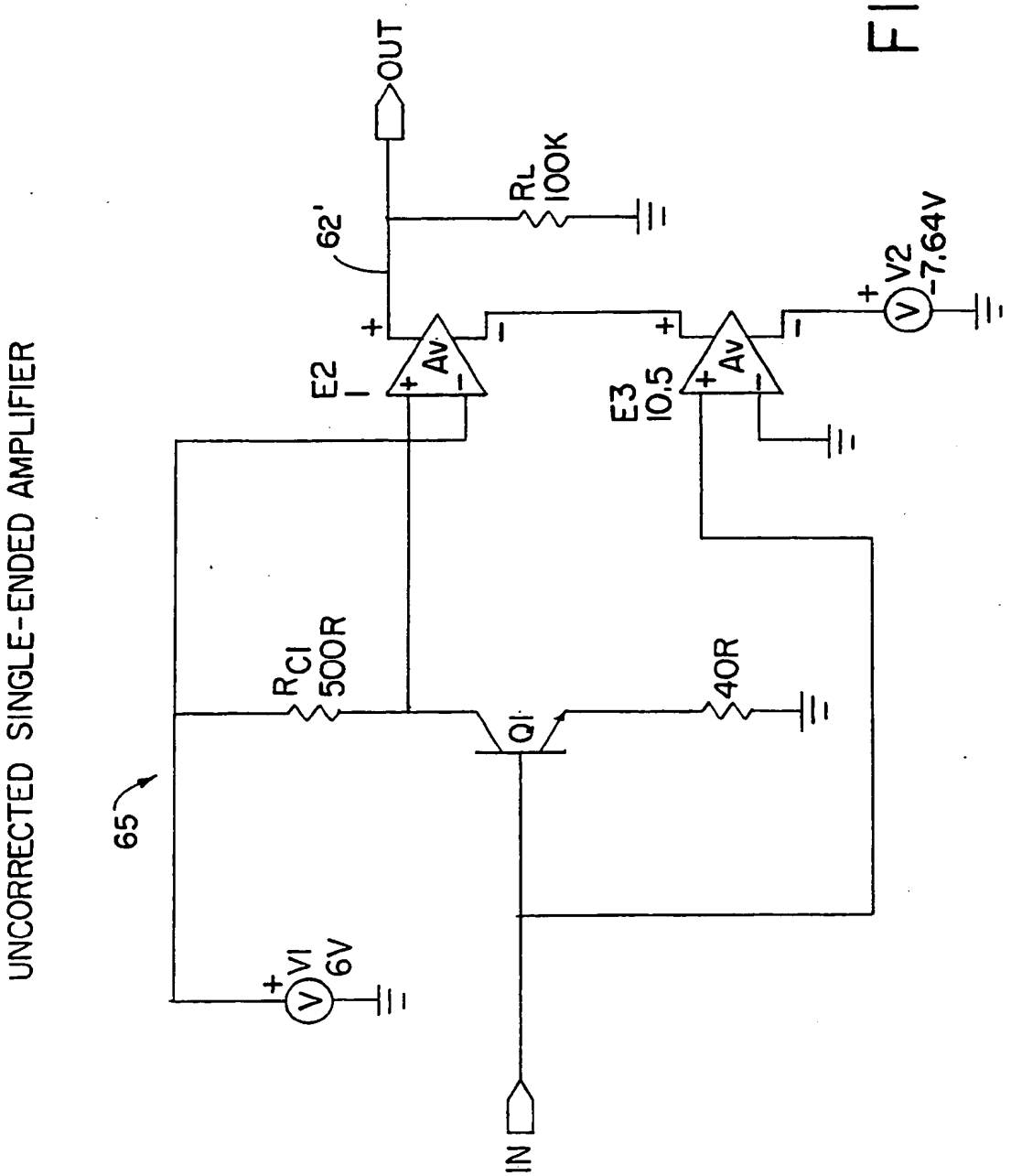

UNCORRECTED SINGLE-ENDED AMPLIFIER
65
OUT
62'
RL
100K
V2
-7.64V
E2
1
Av
E3
10.5
Av
RCI
500R
Q1
40R
V1
6V
IN

FIG. 9

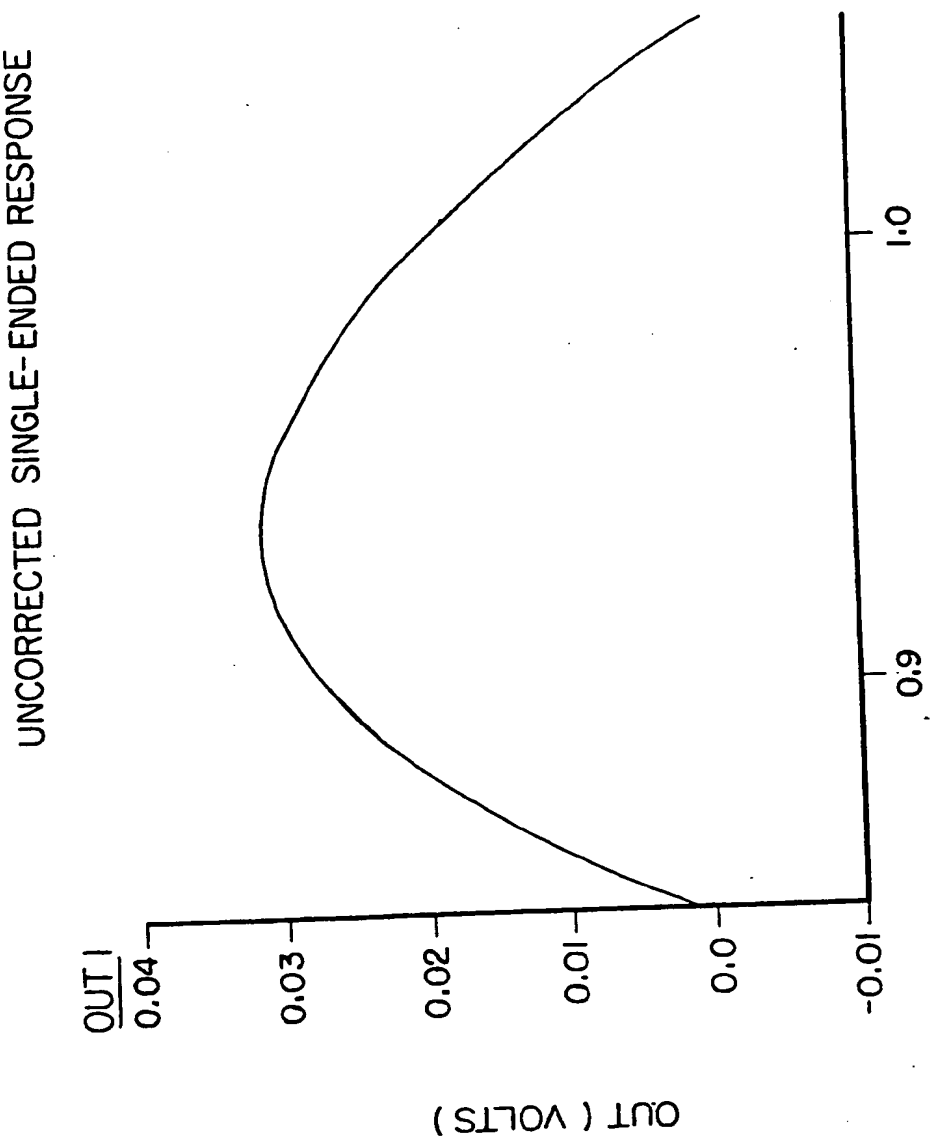

UNCORRECTED SINGLE-ENDED RESPONSE
OUT (VOLTS)
0.04
0.03
0.02
0.01
0.0
-0.01
0.9
1.0
V_{IN} (VOLTS)

FIG. 10

2287370

AMPLIFIER CIRCUIT WITH FEED-FORWARD LINEARITY CORRECTION

Technical Field

The present invention relates generally to amplifier circuits, and more particularly, to amplifier circuits including feed-forward linearity correction.

Background of the Invention

Amplifiers for electrical circuits are well known in the art. For example, differential amplifiers are used extensively as building blocks in modern integrated circuit amplifiers. Fig. 1 illustrates a typical differential amplifier 15. The differential amplifier 15 includes NPN bipolar transistors Q1 and Q2 configured as a differential pair. The base of each transistor Q1 and Q2 represents an input to the differential amplifier 15 for receiving a differential input V_{in}. The collectors of transistors Q1 and Q2 are each connected to a voltage supply +V via resistors R_{C1} and R_{C2}, respectively. The emitters of both transistors Q1 and Q2 are coupled together via resistors R_{E1} and R_{E2}, respectively, and are connected through a current source I_{EE} to a voltage supply -V. A differential output voltage V_{out} is presented across the collectors of Q1 and Q2.

Differential amplifiers such as that shown in Fig. 1 suffer from known disadvantages particularly with respect to linearity of the output V_{out}. As is well known, the response of the differential amplifier 15 is linear only over a limited range of input values applied to the differential input V_{in}. In order to improve the linearity of the differential amplifier response, it is possible simply to increase the operating current through constant current source I_{EE} to an appropriate level. However, there can be further disadvantages associated with attempting to improve linearity simply by increasing the operating current. For example, increasing the operating current can result in a differential amplifier which is less power efficient.

Increasing the operating current also may result in the differential amplifier 15 running at too high a current for optimum gain or frequency response. Moreover, in the event larger transistors Q1 and Q2 are utilized in an effort to optimize gain or frequency response, another problem arises with respect to the increase in capacitance due to the larger transistors. Namely, the increased capacitance can reduce the bandwidth of the differential amplifier.

Another approach for improving linearity of the differential amplifier utilizes conventional feedback techniques. Generally speaking, however, feedback techniques cannot be used to improve linearity at high frequencies due to instability problems.

Still another approach for improving the linearity of a differential amplifier involves the use of feed-forward techniques. More particularly, the error of the main differential amplifier is compensated by an auxiliary amplifier that is even more non-linear. The main differential amplifier error and the auxiliary amplifier error are designed to cancel out each other. Conventional circuit configurations employing such feed-forward techniques are characterized by reduced headroom due to cascading stages, or by requiring substantially increased current and/or power as the amplifier stages are paralleled. Some of these conventional circuit configurations are notable for having most of the input signal applied to the auxiliary amplifier. Other configurations, such as that described in United States Patent 4,146,844 for a "Feed-Forward Amplifier", require matched resistors which either load the input heavily or present a significant impedance to the auxiliary amplifier and thereby limit the bandwidth.

In view of the aforementioned problems associated with known techniques for improving the linearity of an amplifier such as a differential amplifier, it will be appreciated that there is a need in the art for an amplifier having improved linearity. More particularly, there is a need in the art for an amplifier which has improved linearity without sacrificing power efficiency, bandwidth or operating headroom.

Summary of the Invention

According to one particular aspect of the invention, a differential amplifier with feed-forward linearity correction is provided. The differential amplifier includes a main amplifier having a pair of first amplifying devices configured as a differential pair to provide a differential output based on a differential input; a pair of correction amplifiers, each for respectively monitoring a characteristic of one of the main amplifying devices and for providing a linearity correction signal to the differential output as a function of the characteristic; and wherein each of the correction amplifiers includes a pair of second amplifying devices configured as another differential pair, the another differential pair including an input for monitoring the respective characteristic and an output for providing the linearity correction signal.

According to another aspect of the present invention, an amplifier with feed-forward linearity correction is provided including a main amplifier having an amplifying device for providing an amplified output based on an input signal; a correction amplifier for monitoring a characteristic of the amplifying device and for providing a linearity correction signal to the output as a function of the characteristic; and wherein the correction amplifier includes a pair of second amplifying devices configured as a differential pair, the differential pair including an input for monitoring the characteristic and an output for providing the linearity correction signal.

The present invention relates to an amplifier with feed-forward linearity correction. The amplifier advantageously provides a substantially linear response in comparison to conventional amplifier circuits. The amplifier advantageously does not sacrifice power efficiency, bandwidth or operating headroom as is common with other linearity correction techniques.

To the accomplishment of the foregoing and related ends, the invention, then, comprises the features hereinafter fully described and particularly pointed out in the claims. The following description and the annexed drawings set forth in detail certain illustrative embodiments of the invention. These embodiments are indicative, however, of but a few of the various ways in which the principles of the invention may be employed. Other objects, advantages and novel features of the invention will become apparent from the following detailed description of the invention when considered in conjunction with the drawings.

Brief Description of the Drawings

Fig. 1 is a schematic diagram of a conventional differential amplifier;

Fig. 2 is a schematic diagram of a differential amplifier with feed-forward linearity correction including a main amplifier and a pair of correction amplifiers in accordance with the present invention;

Fig. 3 is a schematic diagram of the differential amplifier of Fig. 2 showing exemplary values in accordance with the present invention, and further including output circuitry for providing a linearity error signal;

Fig. 4 is a non-linearity curve for the differential amplifier of Fig. 3 in accordance with the present invention;

Fig. 5 is a schematic diagram of the conventional differential amplifier of Fig. 1 showing exemplary values, and further including output circuitry for providing a linearity error signal;

Fig. 6 is a non-linearity curve for the conventional differential amplifier of Fig. 5;

Fig. 7 is a schematic diagram of a single-ended amplifier with feed-forward linearity correction including a main amplifier and a correction amplifier in accordance with the present invention, and further including output circuitry for providing a linearity error signal;

Fig. 8 is a non-linearity curve for the single-ended amplifier of Fig. 7 in accordance with the present invention;

Fig. 9 is a schematic diagram of a conventional single-ended amplifier, and further including output circuitry for providing a linearity error signal; and

Fig. 10 is a non-linearity curve for the conventional single-ended amplifier of Fig. 9.

Description of the Preferred Embodiments

The present invention will now be described with reference to the drawings, wherein like reference labels refer to like elements throughout.

Referring to Fig. 2, a differential amplifier 20 with feed-forward linearity correction is shown in accordance with the present invention. The differential amplifier 20 includes a main amplifier 22, and a pair of correction amplifiers 23 and 24.

The main amplifier 22 has the same circuit topology as the conventional differential amplifier 15 shown in Fig. 1. The main amplifier 22 includes main transistors Q1 and Q2 (both NPN bipolar transistors) connected as a differential pair with the respective emitters being coupled together via emitter resistors R_{E1} and R_{E2} and connected through constant current source I_{EE} to the -V voltage supply. The collectors of the transistors Q1 and Q2 are coupled to the +V voltage supply by way of collector resistors R_{C1} and R_{C2}, respectively. A differential input V_{in} is provided across the bases of the main transistors Q1 and Q2 via lines 26 and 27, respectively. A differential output V_{out} is presented across the collectors of the main transistors Q1 and Q2 via lines 28 and 29. The output V_{out} can be applied to a load represented by resistor R_L.

The correction amplifier 23 includes a differential pair 32 made up of NPN bipolar transistors Q4 and Q5. The emitters of transistors Q4 and Q5 are coupled directly together and are connected to the -V voltage supply through constant current source I3. The collector of transistor Q4 is connected to the collector of main transistor Q1, and the collector of transistor Q5 is connected to the collector of main transistor Q2. The base of transistor Q5 is connected to the emitter of main transistor Q1, and the base of transistor Q4 is connected to the emitter of diode-connected transistor Q3. The base of transistor Q4 is also connected to the -V voltage supply through constant current source I2. The collector and base of transistor Q3 are connected together and are coupled to the base of main transistor Q1.

The correction amplifier 24 is essentially a mirror image of the correction amplifier 23. The correction amplifier 24 includes a differential pair 35 formed by NPN bipolar transistors Q6 and Q7. The emitters of transistors Q6 and Q7 are coupled together and are connected to the -V voltage supply via a constant current source I4. The collector of transistor Q6 is connected to the collector of main transistor Q1, and the collector of transistor Q7 is connected to the collector of main transistor Q2. The base of transistor Q6 is connected to the emitter of main transistor Q2, and the base of transistor Q7 is connected to the emitter of diode-connected transistor Q8. The base of transistor Q7 is also connected to the -V voltage supply through constant current source I5. The collector and base of transistor Q8 are connected together and are coupled to the base of main transistor Q2.

The operation of the differential amplifier 20 according to the present invention will now be described. As the magnitude of the differential input voltage V_{in} applied across the base of each main transistors Q1 and Q2 is increased, the base-to-emitter voltages (V_{be}) of the main transistors Q1 and Q2 will change. The changes in the V_{be}s of main transistors Q1 and Q2 are due to the changes in the respective collector currents I_{C1} and I_{C2} as is conventional in differential amplifiers.

Ideally, the change in the V_{be}s of the main transistors would be linear with respect to the collector currents I_{C1} and I_{C2} and there would be no resultant linearity error in the main amplifier 22. Realistically, of course, the main transistors Q1 and Q2 are linear in this respect only over a limited range of changes in base-to-emitter voltages. In order to compensate for the non-linearity in the main transistors Q1 and Q2, the present invention

utilizes the correction amplifiers 23 and 24 to monitor the change in V_{be} of the respective main transistors and to compensate for non-linear variations by introducing a correction signal based on the change in V_{be}.

More specifically, each correction amplifier 23 and 24 has as inputs the bases of the transistors in the differential pairs 32 and 35, respectively. The base of transistor Q4 in the correction amplifier 23 is connected to the base of the main transistor Q1 through the diode-connected transistor Q3. The base of transistor Q5 is connected to the emitter of main transistor Q1, and as a result the respective collector currents I_{C4} and I_{C5} through the correction amplifier 23 are a function of the base-to-emitter voltage V_{be} of main transistor Q1. The collector currents I_{C4} and I_{C5} represent a correction signal which, when summed together with collector currents I_{C1} and I_{C2}, respectively, provide a more linear response in the main amplifier 22.

Similarly, the base of transistor Q7 in the correction amplifier 24 is connected to the base of the main transistor Q2 through the diode-connected transistor Q8. The base of transistor Q6 is connected to the emitter of transistor Q2. Thus, the differential pair 35 monitors the V_{be} of transistor Q2 and the resultant collector currents I_{C6} and I_{C7} are a function of the base-to-emitter voltage. The collector currents I_{C6} and I_{C7} of the correction amplifier 24 also combine with the collector current I_{C1} and I_{C2} of the main amplifier 22, respectively, in order to achieve the desired linearity correction.

Since the change in V_{be} of the main transistors Q1 and Q2 is typically very small, it is desirable to offset initially the input to the correction amplifiers 23 and 24 by an amount similar to the quiescent V_{be} of the respective main transistors Q1 and Q2. This is accomplished using the diode-connected transistors Q3 and Q8. More particularly, the constant current through transistor Q3 is selected initially to provide a voltage drop between input line 26 and the base of transistor Q4 equal to the V_{be} voltage of the main transistor Q1, e.g., 700 millivolts. Similarly, the constant current through transistor Q8 is selected initially to provide a voltage drop equal to the V_{be} voltage of the main transistor Q2. As a result, the constant currents through transistors Q3 and Q8 provide a temperature dependent but otherwise fixed voltage drop which quiescently matches the V_{be} voltage of transistors Q1 and Q2, respectively.

In the preferred embodiment, the operating points of the correction amplifiers 23 and 24 deliberately include a further offset on opposite sides of the output response curve

of the main amplifier 22 in order to improve the overall linearity. This offset (on the order of 20 millivolts, for example) is accomplished on the one side for the correction amplifier 23 by establishing a constant current in the diode-connected transistor Q3 (approximately equal to I2) which is different than the quiescent current I_{C1} in the main transistor Q1.

Similarly, an offset is provided on the other side of the correction amplifier 24 by establishing a constant current in the diode-connected transistor Q8 which is different than the current I_{C2} in the main transistor Q2. It is preferred that the size of the transistors Q3 and Q8 be made approximately the same size or larger than the transistors Q1 and Q2, respectively, in order to assist in this offset.

Fig. 3 illustrates the differential amplifier 20 of Fig. 1 including exemplary component values as follows:

I1	=	8 milliamps (mA)	R_{C1}	=	500 ohms
I2	=	1 mA	R_{C2}	=	500 ohms
I3	=	1 mA	R_{E1}	=	44.18 ohms
I4	=	1 mA	R_{E2}	=	44.18 ohms
I5	=	1 mA	R_L	=	100 kilohms
+V	=	6 volts	-V	=	-6 volts

The circuit shown in Fig. 3 also includes an inverter amplifier E1 with unity gain for inverting an input signal $V_{in}/2$ applied to line 26 and having its output connected to line 27. As a result, a differential input voltage V_{in} is applied across lines 26 and 27 as in Fig. 1. For purposes of circuit simulation using the commercially available SPICE software or the like, the circuit of Fig. 3 further includes output amplifiers E2 and E3 designed to produce a linearity error signal on line 40. More specifically, the differential output V_{out} across lines 28 and 29 are input into ideal amplifier E2. The output of amplifier E2 on line 40 is offset by an amount equal to the output of ideal amplifier E3 having a gain (e.g., Av=20) equal to the gain of the differential amplifier 20.

As a result, the output V_{out} from the differential amplifier 20 is subtracted from an ideal linear output provided by amplifier E3 to produce a linearity error signal on line 40 shown in Fig. 4. At an input voltage $V_{in}/2$ equal to 0.0 volts, the linearity error

signal is equal to 0.0 volts. The peak linearity error occurs at approximately $V_{in}/2$ equal to -0.1 and +0.1 volts and is equal to approximately 0.003 volts.

The particular constant current source values I2-I5 are selected by the circuit designer to provide the desired offset relative to the main amplifier 22 in order optimize the linearity error curve (Fig. 4). The particular values and ratios of the various resistances are a function of the performance characteristics of the particular amplifying devices utilized, the desired overall gain of the amplifier 20, and the desired degree of linearity. The particular values and ratios may be determined easily using known circuit simulation techniques, empirical data, etc., as will be appreciated by those having ordinary skill in the art.

It is significant to note in the present invention that the current (approximately 1mA) in the two correction amplifiers 23 and 24 is substantially less than the current (8mA) in the main amplifier 22. For example, the current in each correction amplifier 23 and 24 in the embodiment of Fig. 3 is approximately one-eighth of the current in the main amplifier 22. This is possible because the correction amplifiers 23 and 24 only see the change in V_{be} of the main transistors Q1 and Q2, respectively. Therefore the signal levels involved in the correction amplifiers 23 and 24, and hence the tail current levels, can be quite small.

Accordingly, the correction amplifiers 23 and 24 do not consume large amounts of power and therefore provide linearity correction more efficiently as compared to the above discussed conventional techniques. Moreover, the correction amplifiers 23 and 24 tend to have very little direct effect on the overall bandwidth and pulse response of the differential amplifier 20 as a result of the current through the correction amplifiers being substantially less than the current through the main amplifier 22.

Obviously the collector nodes of the main transistors Q1 and Q2 in the differential amplifier 20 are more heavily loaded with capacitance as compared to a conventional differential amplifier as is shown in Fig. 1. However, this would not cause a significant problem in an actual application of the amplifier 20 since it would be usual to use it in a cascode configuration. Furthermore, the peaking introduced by the extra loading on the emitters of the transistors Q1 and Q2 can more than compensate for the effect of the added capacitance presented at the collectors. It also is possible to use smaller geometry

devices in the correction amplifiers 23 and 24 so that the increase in the collector node capacitance for transistors Q1 and Q2 is not as significant.

The performance of the differential amplifier 20 including linearity correction can be compared with that of a conventional differential amplifier with equivalent gain such as that represented in Figs. 5 and 6. For example, Fig. 5 illustrates the differential amplifier 15 of Fig. 1 including the following exemplary component values:

I_{EE} = 10 mA		R_{C1} = 500 ohms	
+V = 6 volts		R_{C2} = 500 ohms	
-V = -6 volts		R_{E1} = 40 ohms	
R_L = 100 kilohms		R_{E2} = 40 ohms	

The circuit shown in Fig. 5 also includes amplifiers E1-E3 for producing a linearity error signal on line 42 in the same manner as is described above with respect to the circuit of Fig. 3. It will be noted that for purposes of comparison, the values of emitter resistors R_{E1} and R_{E2} in the differential amplifier 15 along with the gain of the ideal amplifier E3 (Av=20.8) are slightly different in order that the overall gain of the amplifier is equal (normalized) to that of the differential amplifier 20 as shown in Fig. 3. Furthermore, the value of the constant current source I_{EE} is set to 10 mA to keep the power level consistent with the differential amplifier 20 in Fig. 3.

Fig. 6 represents the linearity error signal produced on line 42 for the circuit shown in Fig. 5. At an input voltage $V_{in}/2$ equal to 0.0 volts, the error signal is equal to 0.0 volts. The peak linearity error occurs at approximately $V_{in}/2$ equal to -0.1 and +0.1 volts, and is equal to approximately 0.037 volts. Comparing peak linearity errors (e.g., 3 millivolts versus 37 millivolts) the differential amplifier 20 of the present invention provides an improvement in linearity by at least a factor of ten. Notably, such improvement is provided without requiring a substantial increase in power consumption in the amplifier.

It will be appreciated that actual component values provided in Fig. 3 are intended to be illustrative of the present invention and are not intended to limit the scope of the present invention. Different component values can be used in different embodiments of the differential amplifier 20.

Furthermore, although the present invention has been described in the context of using NPN bipolar transistors Q1-Q8 as the amplifying devices, it will be appreciated that other embodiments of the present invention can utilize different amplifying devices such as PNP bipolar transistors, field-effect transistors, etc., or any combination thereof, in place of the transistors Q1-Q8. In the case where field-effect transistors are used in place of bipolar transistors Q1 and Q2, for example, the correction amplifiers can be used to monitor the gate-to-source voltages in the main amplifier.

In addition, with certain circuit configurations using multiple amplifier stages, the diode-connected transistors Q3 and Q8 can be slipped into the previous stage, thereby not increasing the power at all. If, for example, emitter followers are used as inter-stage buffers the diode-connected transistors Q3 and Q8 could be included between the respective emitter follower and its current source. In the event there is too much current in the previous stage emitter follower, the current can be split between the current source of the emitter follower and an auxiliary current source as will be appreciated.

The correction amplifiers 23 and 24 in another embodiment of the present invention may include emitter degeneration. The operating point of the correction amplifiers may be optimized by positioning the current source (e.g., I3, I4) of the respective correction amplifier asymmetrically with respect to the emitter degeneration.

In still another embodiment of the present invention, the amplifying devices (e.g., Q4-Q7) in the correction amplifiers can be of opposite polarity to the amplifying devices (e.g., Q1-Q2) in the main amplifier 22. Furthermore, the correction currents (e.g., I_{C4}-I_{C7}) can be injected into the main amplifier 22 at nodes other than the collector nodes as will be appreciated. A degree of linearity correction can also be achieved when using only one correction amplifier such as correction amplifier 23 and omitting the other correction amplifier 24.

Referring now to Fig. 7, a single-ended amplifier 50 with feed-forward linearity correction is shown in accordance with the present invention. The amplifier 50 includes a main amplifier 22′ and a correction amplifier 23′. The main amplifier 22′ includes a bipolar (NPN) main transistor Q1 having its collector connected to the +V power supply via resistor R_{C1} and its emitter connected to ground via resistor R_{E1}. The base of the transistor Q1 serves as the input to the amplifier 50 via line 55.

The correction amplifier 23′ includes NPN transistors Q4 and Q5 configured in a differential pair 32′. The emitters of transistors Q4 and Q5 are coupled together and are connected to the -V supply through the constant current source I3. The collector of transistor Q4 is connected to the collector of transistor Q1. The collector of transistor Q5, on the other hand, is connected to the +V supply via resistor R. The base of transistor Q4 serves as one input to the differential pair 32′ and is connected to the base of transistor Q1 through diode-connected transistor Q3 (NPN). The base of transistor Q1 is connected to ground through constant current source I2. The base of transistor Q5 serves as the other input to the differential pair 32′ and is connected to the emitter of Q1.

As in the above embodiment of Fig. 2, the correction amplifier 23′ monitors the change in the base-to-emitter voltage (V_{be}) of transistor Q1. Non-linearity errors in the transistor Q1 are compensated for by the addition of the correction current I_{C4} with the main collector current I_{C1}. Again, because the changes in V_{be} will be quite small the diode-connected transistor Q3 is used to offset the input to the correction amplifier 23′. The current in the correction amplifier 23′ can be quite small and therefore will consume very little power since the signal levels in the correction amplifier 23′ are so small. The value of I3 can be used to adjust the gain of the correction current and I2 can be adjusted to control the offset into the correction amplifier 23′.

In the exemplary embodiment of Fig. 7, the output of the amplifier 50 is provided on line 60. Amplifiers E2 and E3 again are combined to compare the output on line 60 with that of an ideal amplifier (E3) to produce a linearity error signal on line 62. The following component values are used in the exemplary embodiment of Fig. 7:

R	=	500 ohms	R_{C1}	=	500 ohms
R_L	=	100 kilohms	R_{E1}	=	44.72 ohms
I2	=	1.5 mA	I3	=	2.0 mA
+V	=	6 volts	-V	=	-6 volts

Fig. 8 represents the linearity error signal response curve for the circuit in Fig. 7 obtained using circuit simulation. It can be seen that a maximum linearity error of approximately 0.0028 volts occurs at an input voltage of approximately 0.95 volts.

Fig. 9 represents a conventional single-ended amplifier 65 without feed-forward linearity correction. The amplifier 65 is similar to the main amplifier 22′ in Fig. 7, except that the value of resistor R_{E1} has been changed in order to provide the same gain as the amplifier 50 for purposes of comparison. Fig. 10 represents the linearity error signal produced on line 62′ of the circuit shown in Fig. 9. It is shown that the maximum linearity error occurs at an input voltage of approximately 0.95 volts and is approximately equal to 0.032 volts. Comparing the curves shown in Fig. 10 and Fig. 8, the single-ended amplifier 50 with feed-forward linearity correction also provides an increase in linearity by at least a factor of ten. Again, such improvement in linearity is achieved without substantially sacrificing power consumption or gain.

As in the case of the differential amplifier 20, the particular currents, resistances, device types, and the ratios of the values in the single-ended amplifier 50 can be selected by the designer to provide the desired degree of linearity correction.

Although the invention has been shown and described with respect to certain preferred embodiments, it is obvious that equivalents and modifications will occur to others skilled in the art upon the reading and understanding of the specification. For example, the present invention has been designed specifically for use in wideband monolithic amplifiers. Nevertheless, the present invention has utility in numerous other applications. In lower frequency applications it is possible to improve the open loop performance of an amplifier using the feed-forward technique of the present invention and further include feedback to give exceptional closed loop performance. Furthermore, the feed-forward technique of the present invention can be combined with various peaking schemes to improve further the performance of the amplifier.

In addition, it will be appreciated that one or both of the correction amplifiers (e.g., 23 and 24) can be used to overcompensate the linearity in the output stage of the amplifier 20 (e.g., Fig. 2) to correct for non-linearities in other stages in a multi-stage amplifier. It will also be appreciated that any or all of the constant current sources described above in connection with the present invention can be replaced by resistors, albeit at the expense of common-mode performance, without departing from the scope of the invention. The present invention includes all such equivalents and modifications.

CLAIMS

1. A differential amplifier with feed-forward linearity correction, comprising:

a main amplifier including a pair of first amplifying devices configured as a differential pair to provide a differential output based on a differential input;

a pair of correction amplifiers, each for respectively monitoring a characteristic of one of said main amplifying devices and for providing a linearity correction signal to said differential output as a function of said characteristic; and

wherein each of said correction amplifiers includes a pair of second amplifying devices configured as another differential pair, said another differential pair including an input for monitoring said respective characteristic and an output for providing said linearity correction signal.

2. The differential amplifier of claim 1, wherein said main amplifying devices are emitter coupled bipolar transistors and said characteristic is a base-to-emitter voltage of said respective transistors.

3. The differential amplifier of claim 2, wherein said outputs of said correction amplifiers are connected to the collectors of said transistors.

4. The differential amplifier of any preceding claim, each of said correction amplifiers further comprising a diode-connected transistor and constant current source connected to said input to offset operation of said correction amplifier relative to said main amplifier.

5. The differential amplifier of claim 4, wherein each of said correction amplifiers are offset in opposite directions relative to said main amplifier.

6. The differential amplifier of any preceding claim, wherein current in said correction amplifiers is substantially less than current in said main amplifier.

7. An amplifier with feed-forward linearity correction, comprising:

a main amplifier including an amplifying device for providing an amplified output based on an input signal;

a correction amplifier for monitoring a characteristic of said amplifying device and for providing a linearity correction signal to said output as a function of said characteristic; and

wherein said correction amplifier includes a pair of second amplifying devices configured as a differential pair, said differential pair including an input for monitoring said characteristic and an output for providing said linearity correction signal.

8. The amplifier of claim 7, wherein said main amplifying device is a bipolar transistor and said characteristic is a base-to-emitter voltage of said transistor.

9. The amplifier of claim 8, wherein said output of said correction amplifier is connected to the collector of said transistor.

10. The amplifier of claim 8 or claim 9, said correction amplifier further comprising a diode-connected transistor and constant current source connected to said input to offset operation of said correction amplifier relative to said main amplifier.

11. The amplifier of any of claims 7 to 10, wherein current in said correction amplifier is substantially less than current in said main amplifier.

12. An amplifier generally as herein described, with reference to or as illustrated in Figures 2 to 10 of the accompanying drawings.

15

Patents Act 1977
Examiner's report to the Comptroller under Section 17
(The Search report)

Application number
GB 9315333.6

Relevant Technical Fields

(i) UK Cl (Ed.L) H3W (WUL, WUP)

(ii) Int Cl (Ed.5) H03F 1/32

Search Examiner
D MIDGLEY

Date of completion of Search
14 OCTOBER 1993

Databases (see below)
(i) UK Patent Office collections of GB, EP, WO and US patent specifications.

(ii) ONLINE DATABASES: WPI, INSPEC

Documents considered relevant following a search in respect of Claims :-
1-11

Categories of documents

X: Document indicating lack of novelty or of inventive step.

Y: Document indicating lack of inventive step if combined with one or more other documents of the same category.

A: Document indicating technological background and/or state of the art.

P: Document published on or after the declared priority date but before the filing date of the present application.

E: Patent document published on or after, but with priority date earlier than, the filing date of the present application.

&: Member of the same patent family; corresponding document.

Category	Identity of document and relevant passages		Relevant to claim(s)
X	GB 2059207 A	(TEKTRONICS) Whole document	7-9, 11
X,&	GB 1572079	(TEKTRONICS) Whole document	7-9, 11
X,&	EP 0259029 A2	(TEKTRONICS) Whole document	7-9, 11
X,&	US 4720685	(TEKTRONICS) Whole document	7-9, 11
X,&	US 4146844	(TEKTRONICS) Whole document	7-9, 11

Databases: The UK Patent Office database comprises classified collections of GB, EP, WO and US patent specifications as outlined periodically in the Official Journal (Patents). The on-line databases considered for search are also listed periodically in the Official Journal (Patents).